

Art Unit: ***

CLMPTO

3/9/04

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CLAIMS 1-6 CANCELLED

1. A method of communicating data in an integrated circuit using internal interconnects, the method comprising:

- receiving a data signal;
- adjusting a first resistance coupled to a first supply voltage, based on a manufacturing process, the first supply voltage and a temperature;
- adjusting a second resistance coupled to a second supply voltage, based on the manufacturing process, the first supply voltage and the temperature; and
- adjusting a third resistance coupled to the second supply voltage, based on the manufacturing process, the first supply voltage and the temperature.

2. A method of communicating data in an integrated circuit using internal interconnects, the method comprising:

- selecting a resistance of a divider network based on a manufacturing process, a supply voltage and a temperature;
- selecting an edge rate of a driver coupled to the divider network, the selected edge rate based on the manufacturing process, the supply voltage and the temperature;
- receiving a data signal; and
- providing an output based on the data signal, the resistance, and the edge rate.

6. The method of claim 5 wherein selecting an edge rate of a driver coupled to the divider network comprises maintaining a substantially constant edge rate.

7. The method of claim 5 wherein providing an output comprises turning on a PFET transistor and turning off an NFET transistor.

8. The method of claim 5 wherein selecting a resistance of a divider network comprises selecting a plurality of parallel resistance elements.

9. The method of claim 5 wherein selecting a resistance of a divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

10. The method of claim 5 wherein selecting an edge rate of a driver coupled to the divider network comprises selecting a plurality of parallel resistance elements.

11. The method of claim 5 wherein selecting an edge rate of a driver coupled to the divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

12. The method of claim 5 further comprising:
receiving a tristate enable signal; and
actuating a switchable resistance element in response to the tristate enable signal.

13. The method of claim 12 wherein actuating a switchable resistance element comprises actuating a programmable inverter.

CLAIMS 17-22 CANCELLED

A1 2

23. [New] The method of claim 7 wherein adjusting a first resistance includes changing a resistance of a semiconductor.

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24. [New] The method of claim 7 wherein adjusting a first resistance includes changing a gate voltage on a field effect transistor (FET).

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25. [New] The method of claim 7 wherein adjusting a first resistance includes selecting a predetermined number of programmable bits from a plurality of programmable bits.